MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2016/2017

ECE2046 – COMPUTER ORGANIZATION AND ARCHITECTURE

(TE/EE/CE/ME/OPE/NANO)

24 FEBRUARY 2017
3:00 p.m – 5:00 p.m.
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This Question paper consists of 6 pages including cover page with 5 Questions only.
2. Attempt **ALL** Questions. The distribution of the marks for each question is given.
3. Please print all your answers in the Answer Booklet provided.

Question 1

(a) Computers have evolved over 5 generations to become what they are today. State ONE (1) defining technology for each of the 5 generations.

[5 marks]

(b) Figure Q1(b) shows the structures of a computer and CPU. Complete the figure by naming the missing components labelled from "A" to "D". Also, briefly state the functions of these components.

[8 marks]

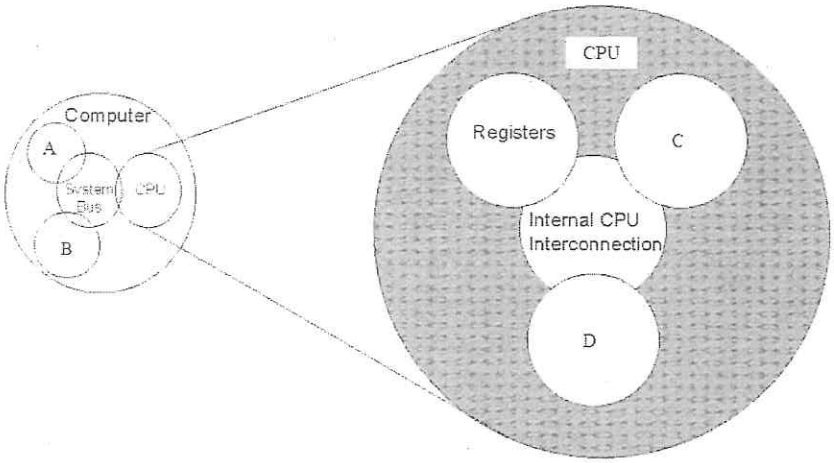

Figure Q1(b)

(c) Given that the number of words in the main memory is 128. Also, given that there are a total of 4 lines in the cache. Furthermore, given that the last 3 bits of the main memory address are used to identify the individual words of each block of memory. Assuming direct mapping function of main memory to cache, calculate:

(i) the size of each block, i.e., the number of words for each block,

[1 mark]

(ii) the number of bits to identify all the lines in cache,

[1 mark]

(iii) the number of blocks in main memory,

[1 mark]

(iv) the number of bits for the tag field of the main memory address.

[1 mark]

(d) State and briefly explain THREE (3) principal techniques for I/O operation.

[6 marks]

(e) Briefly explain the main difference between short I/O wait and long I/O wait.

[2 marks]

Continued...

Question 2

(a) (i) Describe the nature and usage of translation lookaside buffer (TLB).

[2 marks]

(ii) With a neat flowchart, show how page faults are handled in TLB.

[6 marks]

(iii) Describe FOUR (4) advantages of a segmented memory space compared to a non-segmented memory space.

[4 marks]

(b) Differentiate batch multi-programming and time-shared systems by stating their main objectives and the manners of how commands are entered for both these types of systems.

[3 marks]

(c) Define the term swapping in the context of memory management. Explain the need of swapping mechanism.

[2 marks]

Continued...

Question 3

(a) Explain why sign-magnitude representation is seldom put into practical application despite it is one of the simplest ways to represent a signed binary number.

[2 marks]

(b) Solve the following arithmetic operation (the operands are represented as unsigned magnitude) by using the 8-bit two's complement notation. Comment the discrepancies of the result, if any:

(i) $10101110_2 - 111000_2$

[2 marks]

(ii) $10110101_2 + 11000111_2$

[2 marks]

(c) Demonstrate how a computer uses Booth's algorithm to obtain the result of the 6-bit multiplication between 27_{10} and 13_{10}, i.e., $27_{10} \times 13_{10}$.

[4 marks]

(d) Compute the following floating-point arithmetic by assuming that those numbers must be stored in IEEE 32-bit floating-point format:

$$13.125_{10} + 35.625_{10}$$

[7 marks]

Continued...

Question 4

(a) (i) List FOUR (4) examples of types of operands in the context of computer instruction.

[4 marks]

(ii) Given the initial values (in decimal) in the accumulator and assembly code as follow:

A = 10, B = 5, C = 9, D = 3, E = 8

Instruction 1 (I1) : MOV X, A
Instruction 2 (I2) : ADD X, B
Instruction 3 (I3) : MOV Y, D
Instruction 4 (I4) : MUL Y, E
Instruction 5 (I5) : SUB Y, C
Instruction 6 (I6) : DIV Y, X

(I) Determine the number of addresses of I5.

[1 mark]

(II) State TWO (2) characteristics of the addresses in I5.

[2 marks]

(III) Determine the value in decimal of accumulator X after I2 and before I3.

[1 mark]

(IV) Determine the value in decimal of accumulator Y after I4 and before I5.

[1 mark]

(V) Determine the value in decimal of accumulator Y after I6.

[1 mark]

(b) A control unit is made up of numerous inputs and outputs. Answer the following:

(i) Draw a block diagram of the control unit with all its inputs and outputs.

[9 marks]

(ii) List and describe the inputs.

[4 marks]

(iii) List and describe the outputs.

[2 marks]

Continued...

Question 5

(a) Briefly explain the difference between pipelining and superpipelining architectures.

[2 marks]

(b) Multiprocessor and multi-core are two multiprocessing systems. Answer the following:

(i) Using suitable diagrams, illustrate a multiprocessor system and a multi-core system.

[4 marks]

(ii) State and explain THREE (3) advantages of multi-core systems over multiprocessor systems.

[6 marks]

(iii) State and explain ONE (1) advantage of a dual-core system over a single-core system.

[2 marks]

(c) The following programme instructions are referred:

Instruction 1: R3 = R1 + R2
Instruction 2: R4 = R3

(i) Identify the dependency of both of the instructions.

[1 mark]

(ii) Justify your answer in Q5(c)(i).

[1 mark]

End of Paper